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Frequency divide by 8 circuit using T Flip Flop

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# Design Approach:

# The frequency divider by 8 can be obtained by use of T flip flop. The normal circuitry can deploy by interconnecting the initial T flip flop clock with the input clock. The output is then connected with the second flip flops clock and thus resulting into a frequency divided by 4. Similar circuit is continued and the last flip flop receives the clock from the output of the second flip flop. In meanwhile, all the inputs of flip flops are kept as high. As a result the frequency of the clock is divided by 8.

**Source Code:**

module divby8 (output q,input clk,set,clear);

wire q1,q2,nq1,nq2,nq3;

tff1 t1 (nq1,q1,1'b1,clk,set,clear);

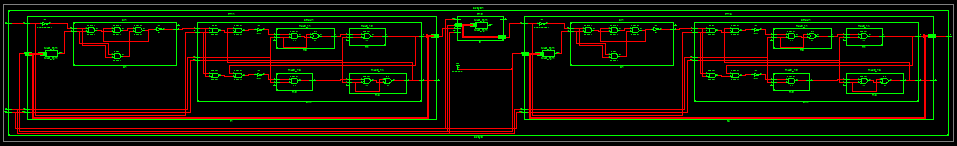
tff1 t2 (nq2,q2,1'b1,q1,set,clear);

tff1 t3 (nq3,q,1'b1,q2,set,clear);

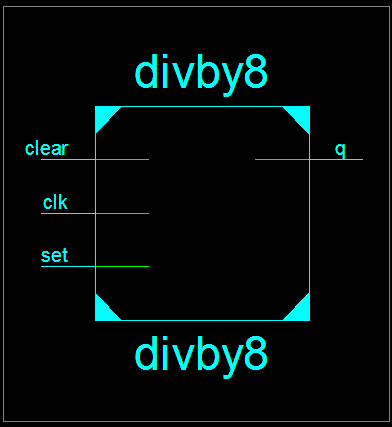
endmodule

**Synthesis:**

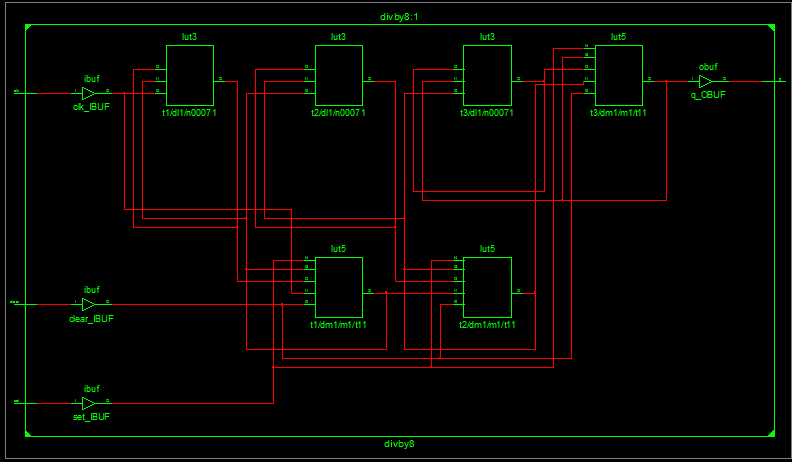
1. RTL Schematic



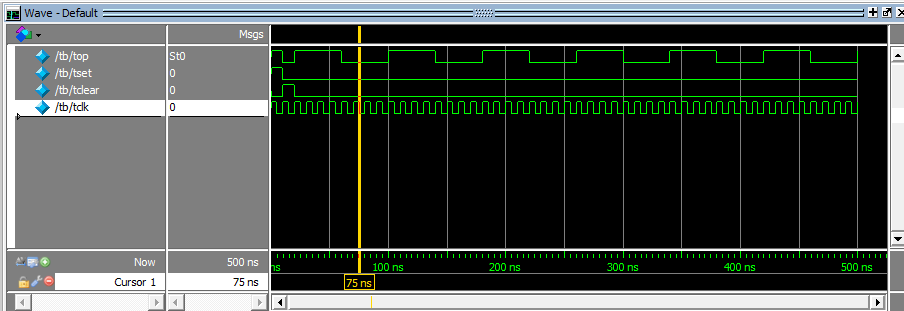
1. Block Diagram

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1. Tech Schematic



1. Simulation Waveform Result

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**Error:**

None.

**Verified by:**

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